



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	4A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	36m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	60m

General Description

Trench Power MV MOSFET technology
High Power and current handing capability
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

PWM application
Load switch

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	4	A
	$T_A=100$		2.5	
Pulsed Drain Current ^A		I_{DM}	20	



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=30V, V_{GS}=0V, T_J=150$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=4A$	-	28	36	m
		$V_{GS}=4.5V, I_D=3A$	-	46	60	
Diode Forward Voltage	V_{SD}	$I_S=4A, V_{GS}=0V$	-	0.9	1.2	V
Gate resistance	R_G					

Typical Electrical and Thermal Characteristics Diagrams

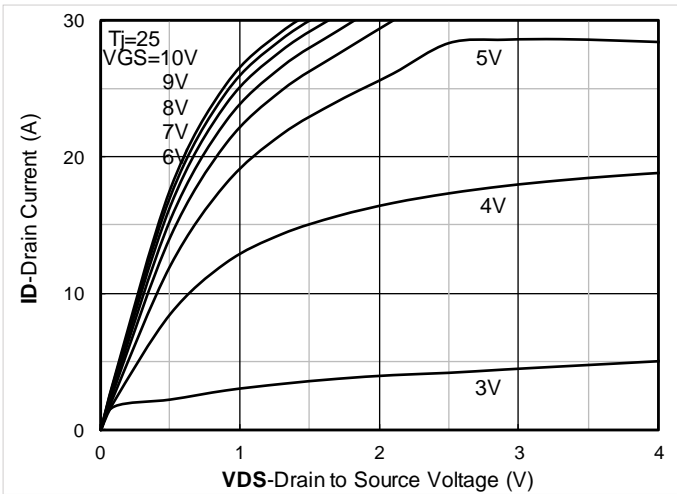


Figure 1. Output Characteristics

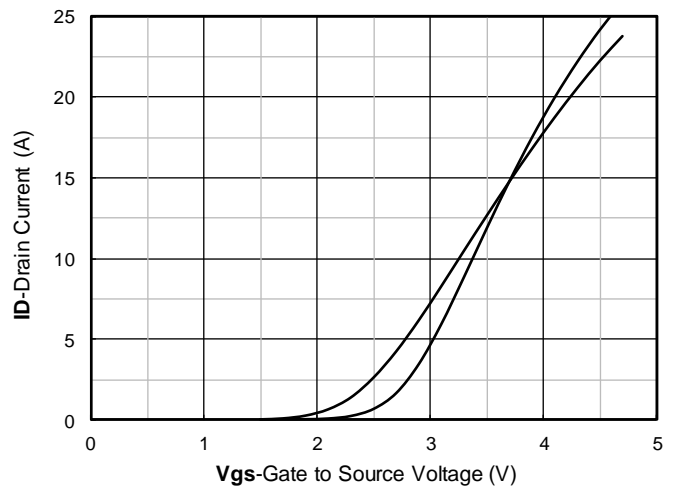


Figure 2. Transfer Characteristics

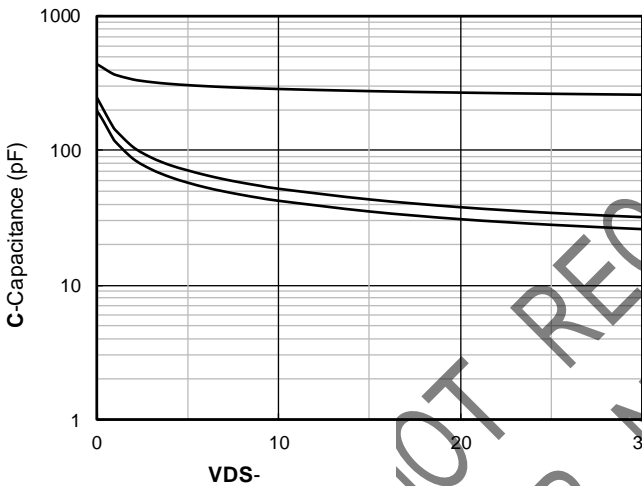


Figure 3. Capacitance Characteristics

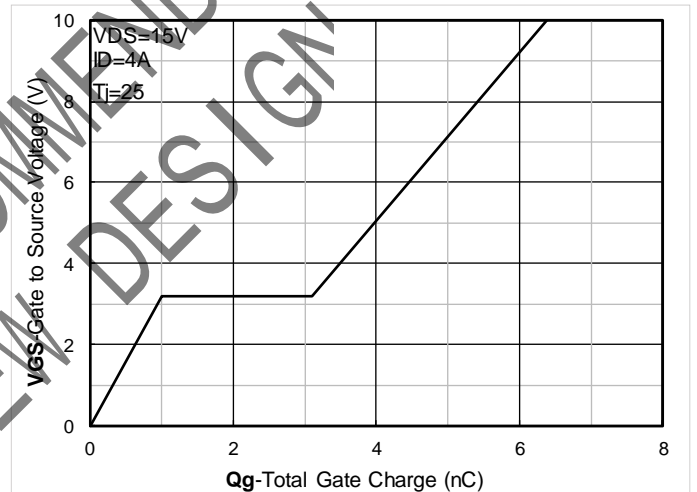


Figure 4. Gate Charge

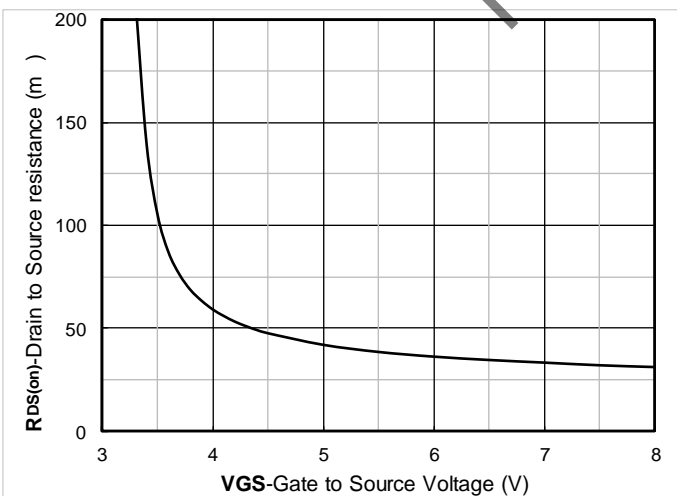


Figure 5. On-Resistance vs Gate to Source Voltage

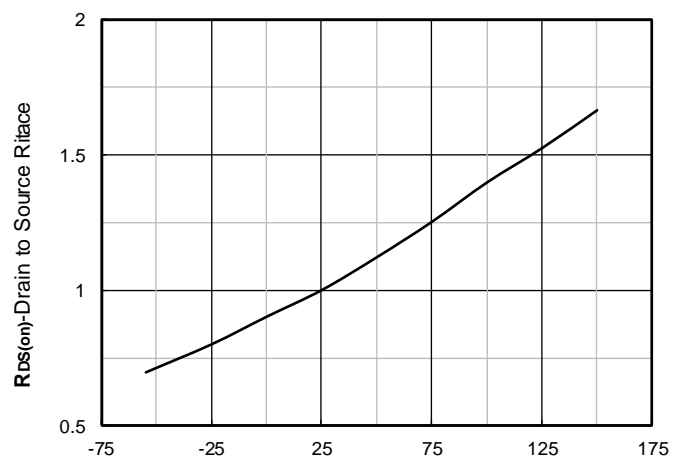


Figure 6. Normalized On-Resistance

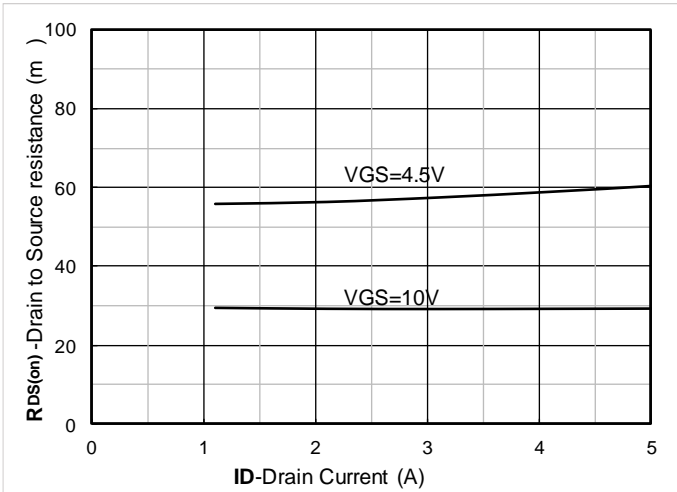


Figure 7. RDS(on) VS Drain Current

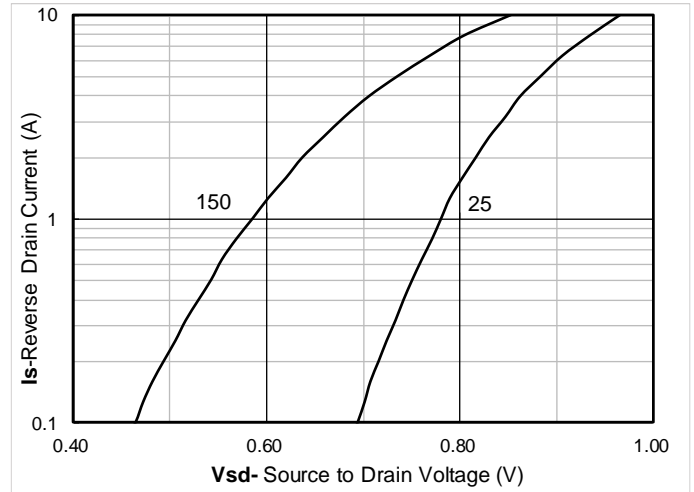


Figure 8. Forward characteristics of reverse diode

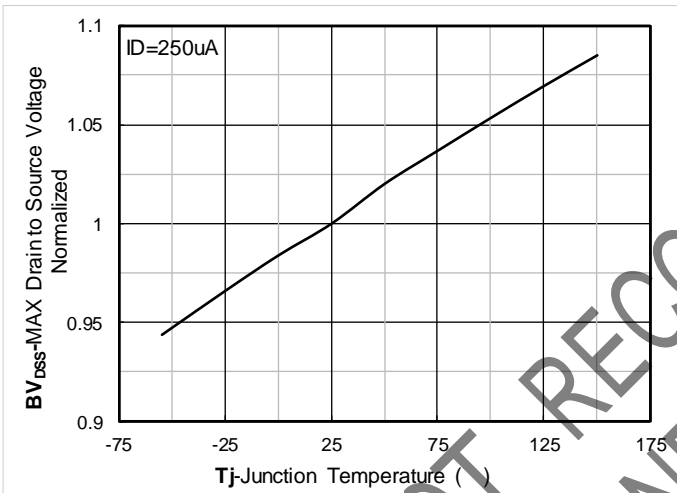


Figure 9. Normalized breakdown voltage

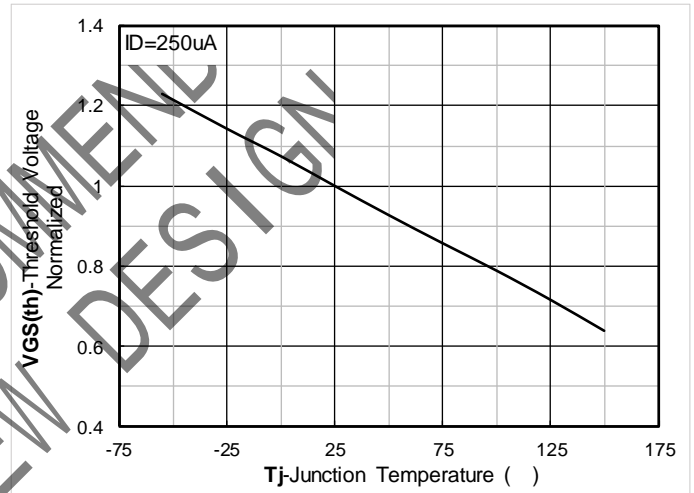


Figure 10. Normalized Threshold voltage

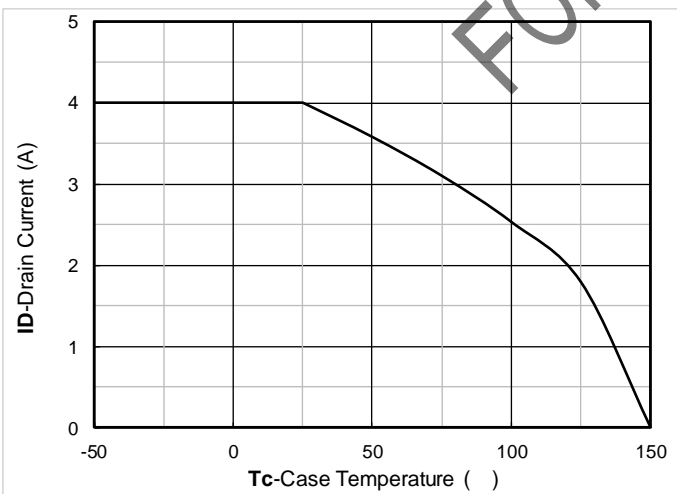


Figure 11. Current dissipation

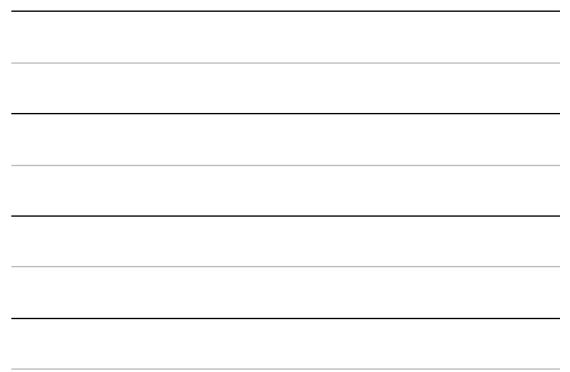


Figure 12. Power dissipation

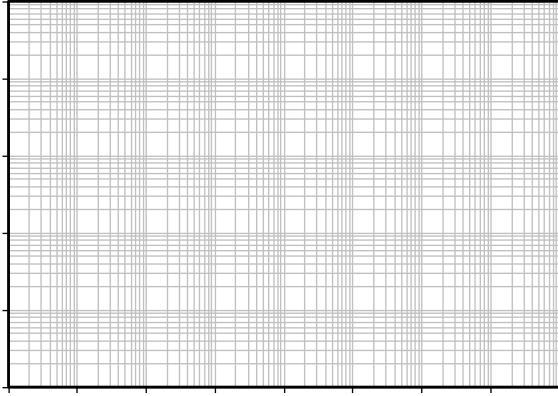


Figure 13. Maximum Transient Thermal Impedance

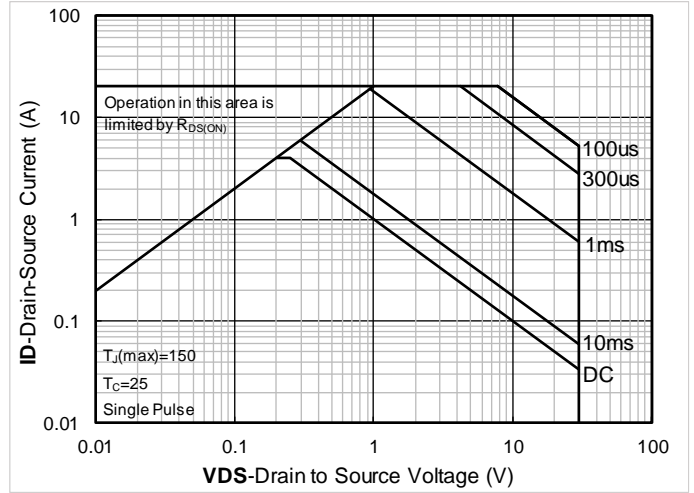


Figure 14. Safe Operation Area

Test Circuits & Waveforms

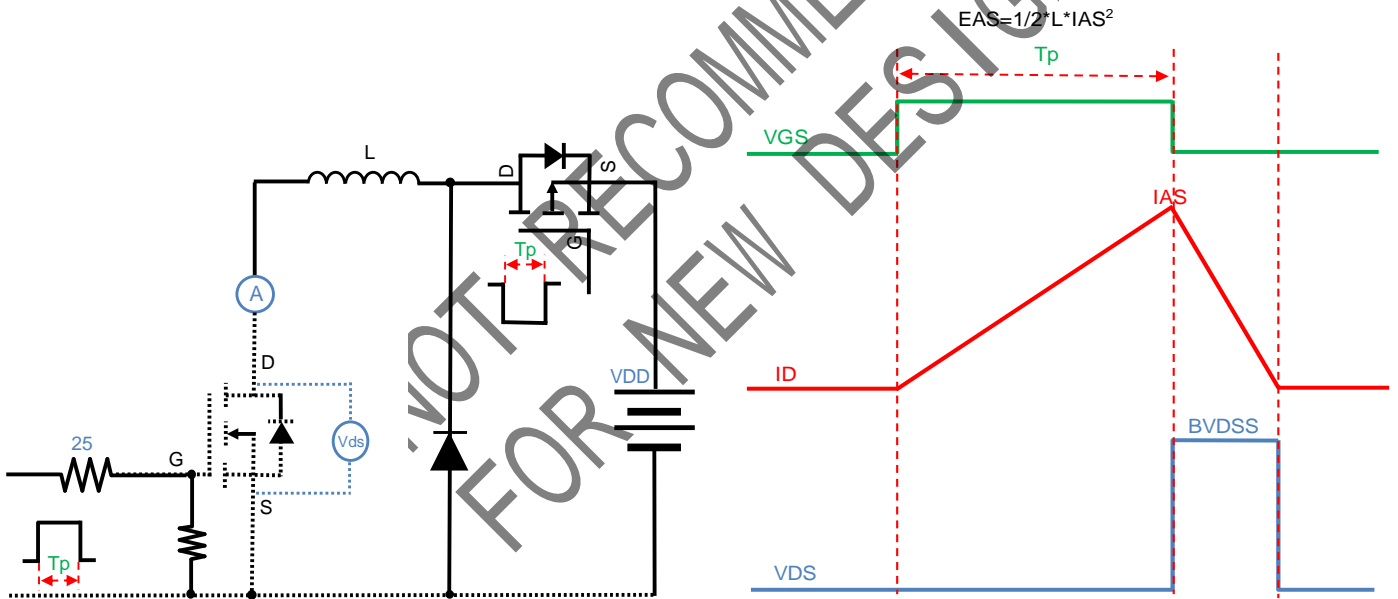
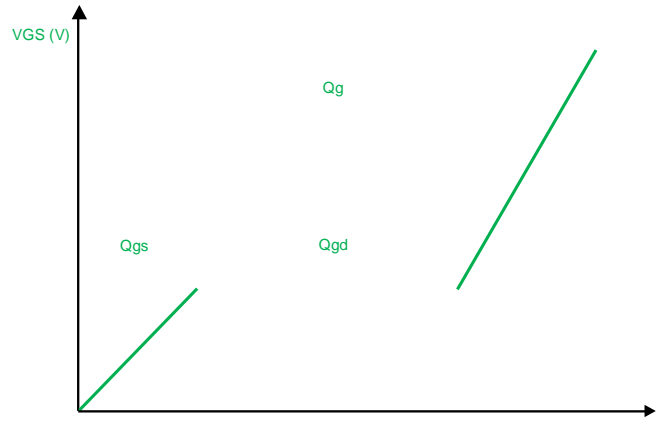
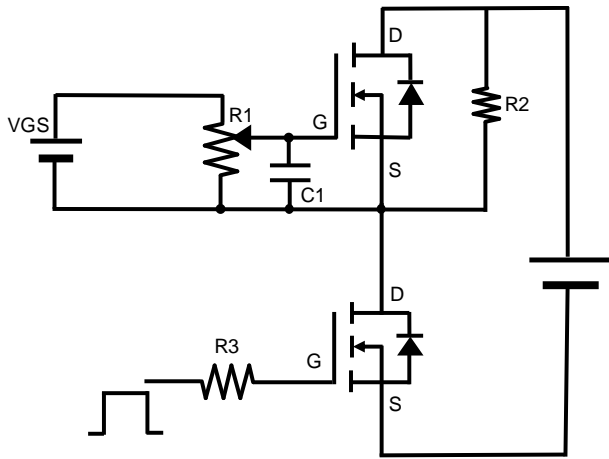


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



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